Reg. date : 16.11.2017

DRB approval date : 3rd DRB dt :

DESIGN & ANALYSIS OF POWER EFFICIENT FLIP FLOP AND ITS APPLICATION IN NANOMETER TECHNOLOGY

SHORT SYNOPSIS

Submitted in partial fulfillment of the requirement of the degree of

DOCTOR OF PHILOSOPHY

to

Manav Rachna International Institute of Research and Studies
(Deemed to be University)

by

Owais Ahmad Shah
Registration number: 17/PhD/037

Under the supervision of
Dr. Geeta Nijhawan
Associate Professor, Faculty of Engineering & Technology

MANAV RACHNA

FACULTY OF ENGINEERING & TECHNOLOGY

MANAV RACHNA INTERNATIONAL INSTITUTE OF RESEARCH & STUDIES

SECTOR-43, SURAJKUND –DELHI ROAD, FARIDABAD – 121001

FACULTY OF ENGINEERING & TECHNOLOGY

Certificate

I hereby declare that the short synopsis "**TITLE: DESIGN & ANALYSIS OF POWER EFFICIENT FLIP FLOP AND ITS APPLICATION IN NANOMETER TECHNOLOGY**" being submitted in partial fulfillment of the requirement for the degree of Doctor of Philosophy in Electronics & Communication Engineering under faculty of Engineering & Technology of Manav Rachna International Institute of Research & Studies, Faridabad during the academic year 2020.

It is a bona fide record of original work carried out under the supervision of Dr Geeta Nijhawan and has not been submitted in full or part to any other university or institute for degree or diploma. Further, it is certified that short synopsis is plagiarism free and proof has been submitted.

Owais

(Owais Ahmad Shah)
Registration number: 17/PhD/037

Geeta

Signature of the Supervisor
Dr Geeta Nijhawan, Assc. Prof., FET, MRIIRS

Signature of the Joint-Supervisor
Dr Imran Ahmed Khan, Assc. Prof, FET, JMI

(Chairman, DRC)

Chairperson, CDP

ABSTRACT

Due to continuous scaling of transistors and increasing requirement of portable equipment, power reduction is of main concern. For design of sequential circuits, flip-flops play very important role. Various existing single edge triggered master slave flip flops and pulse triggered flip flops are examined, simulated, analyzed and optimized in SPICE EDA tool. A novel design will be proposed that consumes low power when compared with the existing literature. The design shall not be only power efficient but area and delay constraints will also to be taken into consideration. The competitiveness of the new design (proposed work) will be shown in terms of power, area and delay with a comparison with existing design. Simulations will also be carried out at different voltage levels to check the viability of the design. Not only voltages, calculations at various data activity (duty cycle) will be obtained for fair comparison and optimum power saving. The proposed work is desired to find application in sequential circuits.

Key words: Switching power, CMOS, power consumption, delay, flip-flops

CONTENTS

S. No.	Description	Page No.
	Certificate	ii
	Abstract	iii
1	Introduction	1-3
2	Literature Review	4-8
	2.1 Gaps in literature	8
3	Description of Work	9
4	Objectives of the Study	10
	4.1 Problem Statement Formulation	10
	4.2 Objective of Research	10
5	Methodology to be adopted	11
6	Expected Outcome of the Research	12
	References	

1. Introduction

Worldwide consumer electronics is growing at a faster pace. Mobile phone in pocket is as powerful as a desktop at home. Power dissipation has become a major concern for semiconductor industry due to increase in complexity of the circuit, speed and density of the device. The requirement for lower power VLSI circuits is driven both by technical needs and businesses.

To achieve low power VLSI circuits following two steps are to be followed:

1. Analysis: for calculations of power dissipation
2. Optimization: the process of generating the best design without violating design specifications.

A Flip-flop is a sequential circuit used for storing binary data. A primary characteristic of sequential logic circuit is the ability to remember the state of the inputs, that is, memory. Two bits which are stored by flip-flops are 1 and 0. A flip-flop circuit is controlled by control flags which are incorporated by clock signals. Flip-flops are bi-stable elements which sample its input data & produce the output data accordingly with respect to a clock edge (P.Joshi et al, 2015). Clock distribution network and flip-flop which are included by clock system are the components which consume highest power that is up to 30% to 60% of the total system power and 90% power consumption is in flip-flops and clock network that is driven by the flip-flop. Mostly edge triggering flip-flop are used as a sequencing element by Application Specific Integrated Circuit (ASIC) design because their timing models are simple (I.A.Khan and M.T Beg, 2013) (S. Kotta and R. Mallavarapu, 2018).

Flip-flop can be categorized as

a] JK flip-flop
b] D flip-flop
c] T flip-flop
d] RS flip-flop

In this study, those flip-flops which belong to D family are discussed. D flip-flop has 1 input that is Data input and the clock input. Data input value is reflected on the Q output when the clock triggered. Therefore, if the D-input is 1, Q output is also 1 and vice versa.

The main applications of flip-flop are listed below (P. Zhao et al, 2004) (J.F. Lin et al, 2017):

a] Data transfer
b] Data storage
c] Counter
d] Register
e] Timer

Flip-flops and latches differed mainly due to the following (V. Stojanovic and V.G. OKlobdzija, 1999):

a] Power consideration
b] Timing

Latches and flip-flops differ in the method used for changing their states. A latch is level sensitive whereas a flip-flop is edge sensitive. Latch is asynchronous i.e. output changes with change in input. Flip-flop's state is changed only when there is transition in control signal because it is edge trigger or synchronous device (C. Lageweg et al, 2004). On reducing the flip-flop power and area, there are following advantages (M.P. Hunglin et al, 2011):-

i. Clock network's power due to lesser clock sinks and lesser capacitive load on clock network.
ii. Limit on skew of clock
iii. Improved routing resource utilization.

Flip-flop is one of the most necessary and indispensable component in designing of digital circuits because its latency is becoming bigger part of cycle time (K.G. Sharma et al, 2011) (F. Keivanian et al, 2016). Types of power in digital electronics system are:

a] Switching (or dynamic) power
b] short circuit power
c] Leakage power (D.M. Kumar and R. Kannusamy, 2017)

In CMOS circuits, approximately 90% power dissipation is because of switching power (J.A. Khan and S.M. Sait, 2007) and in a System-on-chip switching power is 75% of total power consumption (A. Krishnamoorthy , 2004). If 'f' is the rate of charging and discharging of capacitor, the switching power is:

$$P = C_L V^2 f \qquad (1)$$

Where,

C_L = Load capacitance

V = Supply Voltage

In microelectronics, invention of transistor lays down the foundation for low power consuming devices. Therefore, with the invention of IC, performance of the circuits are improved and also led to the reduction of the size of these circuits. In high power consuming devices, silicon failure rate is doubled for every 10℃ rise in temperature (C. Small, 1994). Low power consumption helps to increase device reliability.

Flip-flops have vast applications and as examples can be implemented in:

a] Wireless sensor N/W
b] Smart warehouse
c] Ambient intelligence
d] Wearable computing
e] Smart grids
f] Pollution monitoring
g] Biomedical and implantable device N/W (M. Alioto, 2012).

2. Literature Review

Dashan Pan et al (2019) demonstrated feedthrough flip-flop and named conditional feedthrough pulse triggered flip flop. The advantage of this flip flop was that the power consumption was highly reduced and delay was optimised. Delay optimisation was done using pre discharging and conditional signal feed through scheme. Power was reduced by feedback controlled conditional keeper. At the output node a pull down path was provided to enhance the driving strength. Result of this design also showed higher energy efficiency. The simulation results of this design showed 62% delay reduction when compared to conventional transmission gate flip flop, 66% power efficient and energy efficiency of 87%. All these results demonstrated that the new feed through design is a better option for high efficiency synchronous sequential circuits.

Ahmad Karimi et al (2019) keeping in view the power requirements and scaling factors of day today's fast pacing electronics, pulse triggered CNT FET based D flip flop was investigated. To achieve this, the idea is to reduce the number of transitions occurring between zeros to ones and one's to zeros. Zero to one transition is optimised using signal feedthrough technique, for 1 to 0 transition the discharging path is renewed which reduces the delay, one of the most novel characteristics of this structure is that the pulse generation here does not depend upon the size of the transistor. The simulation result showed great improvements in power dissipation, Delay as well as in the power delay product. Not only this, the number of transistors where are also reduced when compared to the conventional pulse triggered FF.

Chi Yeon Kim and Chul Lee (2019) This letter proposed a readout integrated circuit (ROIC) and uses asynchronous clock gating technique to demonstrate the high dynamic range operation of mid wavelength infrared focal plane arrays. It also uses double edge triggered D flip flop instead of single edge triggered D flip flop in the capacitor reset block. The advantage of using DET D flip flop is that it reduces the error at final output. The input signal and clock signal is controlled by the asynchronous clock gating technique. Using this structure it was observed that the power consumption reduced by 2% when compared to the conventional ROICs. This reduction was observed for low input signal currents.

Pascal A. Meinerzhagen et al (2019) proposed a design which corrects the minimum delay failures. The design also offered 12% to 18% reduction in the dynamic power in 10nm CMOS technology. It was achieved by setting minimum delay margins, error detection and correction for flip flops. The design is ideal for circuits where extreme voltage and technology scaling takes place.

Mojtaba Noorallahzadeh and Mohammad Mosleh (2019) gave a design for efficient energy consumption on reversible computing, which nowadays is an encouraging technology in the field of low power design, optical information processing, nanotechnology, digital signal processing, quantum computing, DNA computing etc. It was found that often the input bits are lost in irreversible circuit, this design proposed reduction in power consumption due to this loss. The design not only emphasized on lower power consumption but also took into consideration the transistor count, the garbage outputs and the constant inputs as well. Eight reversible blocks were analyzed and the result showed these new blocks offered better energy consumption, garbage outputs and constant inputs when compared with the existing previous designs.

Karim Ali et al (2018) proposed to improve designs for spin-orbit torque non volatile flip flop. One is the series programming scheme for spin orbit torque non volatile flip flop and the other is the parallel programming scheme for spin-orbit torque non volatile flip flop. The analysis revealed that parallel programming scheme obtained 29% lesser power and 50% lesser delay when compared with existing parallel architectures. The analysis on series programming scheme revealed 42% lesser power and 52% increase in speed when compared with existing series architecture. In addition to this, both architectures can be used as a function of heavy metal electrode resistance. When taking into consideration the electrode resistance, if the resistance is small then preference is given to series programming scheme because of its speed and energy enhancements and if the resistance is large then the parallel programming scheme is preferred.

Yu-Yun Dai et al (2018) focuses on reduction of dynamic power and accomplishes synthesis and verification of clock gated networks by deriving dependency graph for sequential circuit. Observations showed the properties being expressed as control signals which appeared in dependency graph, are quite easy to show on a clock gated circuit. This design also provided automatic and systematic method for synthesis of sequential clock gating.

A R Palaniappan et al (2018) proposed a flip flop which can operate at an ultra low supply voltage nearly of 0.16 volts and named it capacitively boosted sense amplifier flip flop. This boost is available at the master flip-flop section, a capacitively boosted sense amplifier senses data signal and amplify these data signals to voltage of higher potential than that of supply voltage. By using this, it was observed that the design outperformed most of the flip flops (sense amplifier flip flop) at voltage range of 0.16 to 0.6 volt in terms of delay and power delay product. This flip-flop finds applications in ultra low voltage IoTs, smart modes and wireless sensor nodes.

W A Elsharkasy et al (2017) proposed two designs which improved the reliability of pulsed flip-flops/ latches. Simulations at different voltage levels showed same reliability level. The design compromised the area by around 3% at the cost of negligible power overhead at nominal voltage level when compared to conventional designs at various voltage levels.

Jin-Fa Lin et al (2017) proposed true single phase clocking flip flop using only 19 transistors. It is a hybrid design having both complementary pass transistor logic and static CMOS logic. The design uses logic structure reduction for power and delay performance. In spite of using logic structure reduction there was no floating node seen anywhere. This design also proposed a virtual vdd design for slave latch, enhance delay performance. Seven flip flops where studied and compared in 90nm technology. Proposed design was found to be power efficient with less clock to Q delay and less leakage power consumption. Above all it was found that the design had the smallest area, the area savings was calculated to be approximately equal to 10%.

J Shen et al (2017) proposed a secure design which was an enhanced version of dynamic current mode logic. Dynamic current mode logic has a property of constant power consumption regardless of processed data. It was observed that the proposed full custom flip flop was not only secure but had better PDP. With features like better PDP and higher security this flip flop find applications in ASICs.

StepanLapshev et al (2016) presented five novel static dual edge triggered flip flop which uses C elements and are simulated in the 28nm CMOS technology. When compared with the conventional DET flip flops, novel design showed better characteristics in terms of power delay product and power construction at different switching activities. Among the five novel designs, the low glitch power DET flip flop showed better energy dissipation which in turn is

useful for large logic depth where glitching is more whereas the new conditional toggle DET flip flop was found to have better power delay product and improved power consumption.

S D Pyle et al (2016) introduced a self complementing design which uses only 10 transistors. Simulations where performed in 16nm CMOS technology. The design favoured the area at large but at the cost of higher clock to Q delay. The design was also power efficient.

Jin-Fa Lin et al (2015) gave low power sense amplifier based flip flop. The sense amplifier used as single ended pass transistor, the simulations of which showed improvements in power consumption and low complexity.

Y Junki et al (2015) proposed a stacked leveling critical charge flip flop in a process known as silicon on thin Box (SOTB). This flip-flop was a radiation hardened non-redundant flip-flop. At a particular supply voltage (0.4v) this flip flop was seen to be 27 times stronger than the conventional D flip flop. It was also observed that this flip-flop maintained smaller delay and consume less power when compared with standard D flip flop.

I A Khan et al (2013) used conditional feedback which reduced the short circuit current and decreased the number of clock transistor for power reduction. Simulations yielded improvements of upto61.82% and 55.74% in PDP and power consumption at the price of small increase in area.

K Singh et al (2012) gave a static master slave flip flop, the configuration of which was based on feedback loop, regenerative, using pass transistor. In this number of transistors where drastically reduced to 11 only. The design also achieved 16 % power improvement when compared with conventional design at 250MHz. Such flip-flops found places in microcontroller and microprocessor.

Uming Ko et al (2000) energy, power and performance of few single edge triggered master slave D flip flops are investigated and two new designs were proposed. A push pull D flip flop and a push pull isolation D flip flop. These two new designs were found to be energy efficient and fastest among all the investigated flip flops. It was observed that the power dissipation in push-pull D flip flop was improved by 1% and delay was improved by 31% when compared to conventional D flip flop, whereas the push-pull isolation D flip flop was 45% to 122% energy efficient.

G Gerosa et al (1994) proposed a single edge triggered master slave flip flop (a part of larger circuitry RISC microprocessor) whose speed was optimised by the following: All the

bit inputs were from CMOS logic; feedback of the latch was open electrically while in write operation & the scan operation was multiplexed in latch using a separate clock.

2.1 Gaps in Literature:

Following are the gaps found in existing literature:

a. Multiple inverters are used in various designs to form the pulse, giving rise to power.
b. The D-to-Q delay is large. Longer delays are observed in maximum existing designs.
c. Multiple floating nodes are observed in few structures when the input data and output data both are "1" resulting in additional dc power dissipation.
d. Extra pMos in some designs produces short duration currents.

3. Description of Work

Power dissipation in VLSI chip became a parameter that cannot be ignored nowadays. Frequency and density of a device where some factors which were low in the past, but now since the evolution of Ultra Large Scale Integration (ULSI) more and more transistors are packed in a chip increasing packaging density. The increased device density and operating frequency resulted in higher power dissipation. At present there stands no slowdown in the growth of processing technology. Needless to mention the growth of consumer electronics from the past 10 to 15 years where battery powered mobile phones and laptops have seen tremendous success. A light weighted, compact and efficient product with higher battery life is the need of the hour.

Flip flops are the basic storage elements bistable in nature, sample input data and produces output data at a given clock. There are many designs of D flip flop available; some designs are efficient at power whereas some are faster i.e. with less delay. Some designs are area-efficient as well. In this research, existing D flip flop designs will be studied, analysed and simulated in SPICE tool. Nanometre technology will be adopted for all the simulations. Various parameters like power, delay, Power Delay Product (PDP) of these designs with variation of supply voltage and temperature will be obtained. A novel D flip-flop design will be proposed. Again various parameters of this new design with variations in temperature and supply voltage will be obtained. The results of the novel design will then be then compared with the existing designs which should show the capability of new design to be a viable option for the sequential circuits.

4. Objectives of the Study

4.1 Problem Statement Formulation:

Low power and energy efficient circuits are important in today's fast pacing consumer electronics and next generation processors. The integration scale of electronics increases over predecessors and more and more transistors are packed inside chips than ever before. Flip flop being the basic storage element yields estimated 80% of clock power.

This research intends to find a novel flip flop structure that consumes lesser power and is delay efficient when compared to existing available designs. The goal is to try and reach to an ideal design without compromising area, delay and efficiency.

4.2 Objectives of Research:

a. Analyze and optimize the existing designs.

b. To propose a design that consumes low power when compared with the existing literature.

c. The design should not be limited to low power but low area and less delay also to be taken into consideration.

d. To show the competitiveness of the new design in terms of power, area, Power Delay Product (PDP) and delay when compared with existing designs.

5. Methodology

a. Existing flip flop designs will be simulated in EDA SPICE tool in nanometre technology.

b. Power, delay, area of these existing architectures will be obtained.

c. A novel power efficient flip flop to be proposed.

d. The novel design will be compared with existing flip flop design for different parameters like voltage level, duty cycle, technology etc. The performance comparison of all flip flop structures will be obtained. The power consumption of the flip-flop structures with the variation of temperature and supply voltage will be achieved. The delay and PDP (Power delay Product) of these structures with the variation of temperature and supply voltage will be analyzed.

e. The proposed design will be checked for suitable practical applications.

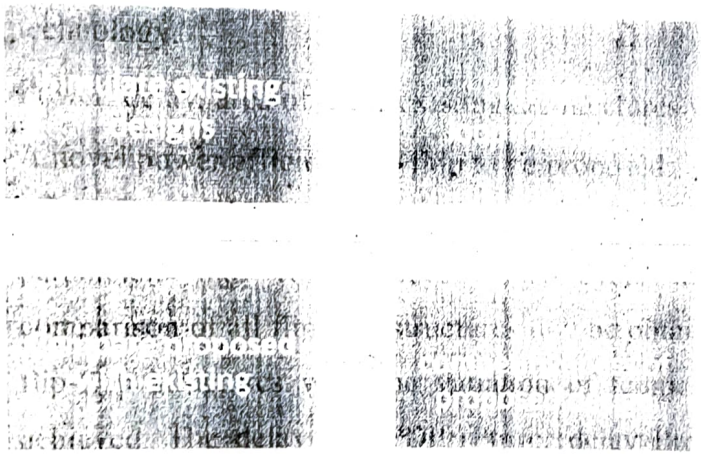

Figure 1: Methodology

6. Expected Outcome of Research

A novel power efficient D-flip flop will be proposed. The design is intended to be a viable option for sequential circuits. The performance parameters of the proposed design to outperform the existing designs.

References

A. Karimi, A. Rezai and M. M. Hajhashemkhani, "Ultra Low Power Pulse-Triggered CNTFET-Based Flip Flop", *IEEE Transactions on Nanotechnology*, Vol. 18, pp 756-761, 2019.

A. Krishnamoorthy, "Minimize IC power without sacrificing performance", *EE Times*, Jul. 15, 2004.

A. R. Palaniappan and L. Siek, "Wide-input dynamic range 1 MHz clock ultra-low supply flip-flop," *Electronics Letters*, vol. 54, no. 15, pp. 938-939, 12 Jun. 2018.

C. Lageweg, S. Cotofana and S. Vassiliadis, "Single Electron Encoded Latches and Flip-Flops, *IEEE Transations on Nanotechnology*, Vol. 3, No. 2, PP. 237-248, June 2004.

C. Small, "Shrinking Devices Put the Squeeze on System Packaging", *EDN*, Vol. 39, No. 4, pp. 41-46, Feb. 17, 1994.

C. Y. Kim and H. C. Lee, "Low-Power, High-Sensitivity Readout Integrated Circuit With Clock-Gating, Double-Edge-Triggered Flip-Flop for Mid-Wavelength Infrared Focal-Plane Arrays", *IEEE Sensors Letters*, Vol. 3, No. 9, pp. 1-4, 2019.

D. Pan, C. Ma, L. Cheng, and H. Min, "A Highly Efficient Conditional Feedthrough Pulsed Flip-Flop for High-Speed Applications", *IEEE Trans. Very Large Scale Integr. (VLSI) System*, Vol. 28, pp 243–251, 2019.

D.M. Kumar and R. Kannusamy, "An Efficient Design of Low Power Sequential Circuit using Clocked Pair Shared Flip- Flop", *International Journal of Applied Engineering Research*, ISSN 0973-4562 Vol. 12, No. 2, pp. 233-237, 2017.

F. Keivanian, N. Mehrshad and A. Bijar, "Multi-objective optimization of MOSFETs channel widths and supply voltage in the proposed dual edge-triggered static D flip-flop with minimum average power and delay by using fuzzy non-dominated sorting genetic algorithm-II", *SPRINGER Plus*, pp.1-15, 2016.

G. Gerosa, S. Gary, C. Dietz, D. Pham, K. Hoover, J. Alvarez, H. Sanchez, P. Ippolito, T. Ngo, S. Litch, j. Eno, J. Golab, N. Vanderschaff and J. Kahle, "2.2W, 80MHZ

superscalar RISC Microprocessor," *IEEE Journal of Solid-State Circuits*, Vol. 29, No. 12, pp. 1440-1454, Dec. 1994.

I.A. Khan and M.T. Beg, "Design and Analysis of Low Power Master Slave flip-flops", *Informacije •MIDEM Journal of Microelectronics, Electronics Components and Materials*,Vol. 43, No.1, pp.41-49, 2013.

I.A. Khan and M.T. Beg, "New Single Edge Triggered Flip-Flop Design with improved Power and Power Delay Product for Low Data Activity Applications" *World Applied Sciences Journal (WASJ)*, ISSN 1818-4952, Volume 22, No. 10, pp. 1520-1526, 2013.

J. F. Lin, Y. T. Hwang, C. S. Wong and M. H. Sheu, "Single-ended structure sense-amplifier-based flip-flop for low-power systems", *Electron. Lett.*, Vol. 51, No. 1, pp 20–21, 2015.

J. Furuta, J. Yamaguchi and K. Kobayashi, "A radiation-hardened non-redundant flip-flop stacked leveling critical charge flip-flop in a 65 nm thin BOX FD-SOI process", *IEEE Trans. Nucl. Sci.*, vol. 63, no. 4, pp. 2080-2086, Aug. 2016.

J. Shen, L. Geng and F. Zhang, "Dynamic current mode logic based flip-flop design for robust and low-power security integrated circuits", *Electron. Lett.*, vol. 53, no. 18, pp. 1236-1238, Aug. 2017.

J.A. Khan and S.M. Sait, "Fast Fuzzy Force-Directed/Simulated Evolution Meta heuristic for Multi objective VLSI Cell Placement", *The Arabian Journal for Science and Engineering*, Vol. 32, No. 2B, pp. 263-280, 2007.

J.F. Lin, M.H. Sheu, Y.T. Hwang, C.S. Wong, and M. Y. Tsa, "Low-Power 19-Transistor True Single-Phase Clocking Flip-Flop Design Based on Logic Structure Reduction Schemes" *IEEE Transactions on Very Large Scale Integration (VLSI) Systems 1*, pp. 1-12, 2017.

K Ali, F Li, S Y H Lua and C-H Heng, "Energy- and area-efficient spin-orbit torque nonvolatile flip-flop for power gating architecture", *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 26, pp. 630-638, 2018.

K Singh, S.C. Tiwari and M. Gupta, "A Master-Slave Flip-Flop for Low Voltage Systems with Improved Power- Delay Product," *World Applied Sciences Journal*, Vol.16 (Special Issue on Recent Trends in VLSI Design), pp. 45-52, 2012.

K.G. Sharma, T. Sharma, B.P. Singh and M. Sharma " Modified SET D-Flip-Flop Design for low Power VLSI Application", *IEEE International Conference on Devices and Communications (ICDeCom)*, 2011.

M. Alioto, "Ultra-Low Power VLSI Circuit Design Demystified and Explained, A Tutorial", *IEEE Transactions on Circuits and Systems-I*, Vol. 59, No. 1, PP. 3-29, Jan. 2012.

M. Noorallahzadeh and M. Mosleh, "Efficient designs of reversible latches with low quantum cost," *IET Circ Device Syst*, vol. In Press, 2019.

M.P. Hunglin, C.C. Hsu and Y.T. Chang, "Recent Research in Clock Power Saving with Multi- Bit Flip-Flop"s, *IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1-4, 2011.

P. A. Meinerzhagen, S. Kunda, A. Malavasi, T. Nguyen, M. M. Khellah, J. W. Tschanz and V. De, "Min-Delay Margin/Error detection and Correction for Flip Flops and Pulsed Latches in 10-nm CMOS", *IEEE Solid State Circuits Letters*, Vol. 2, No. 9, pp. 147-150, 2019.

P. Joshi, S. Khandelwal and Akash "Implementation of low power flip-flop in Nanometer Regime", *IEEE, 2015 Fifth International Conference on Advanced Computing & Communication Technologies (ACCT)*, PP.252-256, 2015.

P. Zhao, T.K. Darwish and M.A. Bayoumi, "High Performance and Low- Power Conditional Discharge flip flop", *IEEE Transaction on Very Large Scale Integration (VLSI) System*, Vol. 12, No. 5, PP. 477-484, 5 May, 2004.

S. D. Pyle, H. Li, and R. F. DeMara, "Compact low-power instant store and restore D flip-flop using a self-complementing spintronic device", *Electron Lett*, Vol. 52 No. 14 pp. 1238–1240, 2016.

S. Kotta and R. Mallavarapu, "Novel Design of Pulse Trigger Flip- Flop with High Speed and Power Efficiency" *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications, Spranger Lecture Notes in Electrical Engineering 434*, pp. 239-246, 2018.

S. Lapshev and S. R. Hasan, "New low glitch and low power DET flip-flops using multiple C-elements", *IEEE Trans. Circuits Syst. I*, Vol. 63, pp 1673–1681, 2016.

U. Ko and P.T. Balsara, "High-Performance Energy-Efficient DFlip-Flop Circuits," *IEEE Transaction on Very Large Scale Integration (VLSI) Systems*, Vol. 8, No. 1, pp. 94-98, 2000.

V. Stojanovic and V.G. OKlobdzija, "Components Analysis of Master Slave Latches and flip-flops for High-Performance and Low power systems" *IEEE Journal of Solid -State Circuits*, Vol. 34, No. 4, pp.536-548, April 1999.

W. M. Elsharkasy, A. Khajeh, A. M. Eltawil and F. J. Kurdahi, "Reliability enhancement of low-power sequential circuits using reconfigurable pulsed latches", *IEEE Trans. Circuits Syst. I Reg. Papers*, vol. 64, no. 7, pp. 1803-1814, Jul. 2017.

Y. Y. Dai and R. K. Brayton, "Verification and synthesis of clock-gated circuits", *IEEE Trans. Comput.-Aided Design Integr.*, pp. 366-379, Feb. 2018.

MANAV RACHNA
vidyaprantarikshan

Dr. O.P. Bhalla Central Library
Manav Rachna International Institute of Research and Studies
(A deemed-to-be-university under section 3 of UGC Act 1956)

SIMILARITY VERIFICATION CERTIFICATE

Title: Design & Analysis of Power Efficient flip-flop and its Application in Nanometer Technology

Researcher: Owais

Registration Number: 17/PhD/037

Supervisor: Dr. Geeta Nijhawan

Department: ECE

This is to certify that the above mentioned Short Synopsis/~~Thesis~~ was scanned for similarity index through Turnitin Software on. 12.10.2020 with submission ID 1412998872 and the similarity index was found to be 8 %. The complete report running into 20 Pages, 4254 Word count with File Size 211.7 KB is being forwarded to the Research Supervisor/DRC/DRB for review.

Date: 12.4.2021

The complete report of the above Short Synopsis/~~Thesis~~ has been reviewed and the similarity index is below the accepted norms as per the University Grants Commission (Promotion of Academic Integrity and Prevention of Plagiarism in Higher Educational Institutions) Regulations 2018. The Short Synopsis/Thesis may be considered for further processing.

for Jyoti
Research Supervisor

Research Scholar

Owais_Ahmad_Shah,_Short_Synopsis_12.10.2020

by Owais_ahmad Shah1

Submission date: 12-Oct-2020 10:11PM (UTC+0530)
Submission ID: 1412998872
File name: Owais_Ahmad_Shah,_Short_Synopsis_FET_October_11_2020.docx (49.6K)
Word count: 4254
Character count: 22651

DESIGN OF POWER EFFICIENT FLIP FLOP AND ITS APPLICATION

SHORT SYNOPSIS

by

Owais Ahmad Shah
Registration number: 17/PhD/037

Under the supervision of
Dr. Geeta Nijhawan

ABSTRACT

Due to continuous scaling of transistors and increasing requirement of portable equipment, power reduction is of main concern. For design of sequential circuits, flip-flops play very important role. Various existing single edge triggered master slave flip flops and pulse triggered flip flops are examined, simulated, analyzed and optimized in SPICE EDA tool. A novel design will be proposed that consumes low power when compared with the existing literature. The design shall not be only power efficient but area and delay constraints will also to be taken into consideration. The competitiveness of the new design (proposed work) will be shown in terms of power, area and delay with a comparison with existing design. Simulations will also be carried out at different voltage levels to check the viability of the design. Not only voltages, calculations at various data activity (duty cycle) will be obtained for fair comparison and optimum power saving. The proposed work is desired to find application in sequential circuits.

Key words: Switching power, CMOS, power consumption, delay, flip flops

Owais_Ahmad_Shah,_Short_Synopsis_12.10.2020

ORIGINALITY REPORT

Exclude quotes On
Exclude bibliography On
Exclude matches less than 25 words

8% SIMILARITY INDEX

3% INTERNET SOURCES

9% PUBLICATIONS

2% STUDENT PAPERS

12/4/21

MATCH ALL SOURCES (ONLY SELECTED SOURCE PRINTED)

2%

★ Imran Ahmed Khan, Owais Ahmad Shah, Mirza Tariq Beg. "Analysis of different techniques for low power Single Edge Triggered Flip Flops", 2011 World Congress on Information and Communication Technologies, 2011

Owais_Ahmad_Shah,_Short_Synopsis_12.10.2020

/0

Instructor